AMENDMENTS TO THE SPECIFICATION

Amend the specification by inserting before the first line the sentence:

This is a continuation of Application No. 10/203,405 filed August 9, 2002, which is a

National Stage Application filed under §371 of PCT Application No. PCT/JP01/11020 filed

December 17, 2001; the above noted prior applications are all hereby incorporated by reference.

On page 50, please replace the second full paragraph, with the following amended

paragraph:

When the elapsed time is 8/32 MHz (at the timing T2 of fb), the pulse number set value

Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14

latches the output $\theta 2$ immediately before (elapsed time = 7/32 MHz) and the output value $\theta 1$

thereof becomes $\theta 1 = 32$ MHz. The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the

overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 32$ MHz + 8 MHz

= 40 MHz, since the overflow signal is $\cancel{1}\underline{0}$. The output value fd of the pulse generation circuit

17d is fd = 0, since $D1 \leq \theta 2 < (D2 \times 3)$, and the second data holding circuit 18 latches the value

fd (= 0) immediately before and the output value fout thereof becomes fout = 0.